CLAIMS:

The invention claimed is:

1. A method of forming a capacitor, comprising:

forming a first capacitor electrode over a semiconductor substrate;

forming a capacitor dielectric region onto the first capacitor electrode, the capacitor dielectric region comprising an exposed oxide containing surface;

treating the exposed oxide containing surface of the capacitor dielectric region with at least one of a borane or a silane; and

depositing a second capacitor electrode over the treated oxide containing surface, the second capacitor electrode comprising an inner metal surface contacting against the treated oxide containing surface.

2. The method of claim 1 wherein the first capacitor electrode consists essentially of semiconductive material.

3. The method of claim 1 wherein the first capacitor electrode consists essentially of metal.

4. The method of claim 1 wherein the exposed oxide containing surface comprises hafnium oxide.

5. The method of claim 1 wherein the exposed oxide containing surface comprises aluminum oxide.

6. The method of claim 1 wherein the treating is with at least one borane.

7. The method of claim 6 wherein all borane used during the treating is void of halogen.

8. The method of claim 6 wherein the borane is selected from the group consisting of BH_3, B_2H_6, B_4H_{10}, B_5H_9, B_6H_{10} and $B_{10}H_{14}$, and mixtures thereof.

9. The method of claim 1 wherein the treating is with at least one silane.

10. The method of claim 9 wherein all silane used during the treating is void of halogen.

11. The method of claim 9 wherein the silane is selected from the group consisting of SiH_4, Si_2H_6, Si_3H_8 and Si_4H_{10}, and mixtures thereof.

12. The method of claim 1 wherein any layer deposited by the treating is no more than 3 monolayers thick.

13. The method of claim 12 wherein no layer is deposited by the treating.

14. The method of claim 1 wherein the exposed oxide containing surface comprises hafnium oxide, and wherein any layer deposited by the treating is no more than 3 monolayers thick.

15. The method of claim 1 wherein the exposed oxide containing surface comprises aluminum oxide, and wherein any layer deposited by the treating is no more than 3 monolayers thick.

16. The method of claim 1 wherein the treating comprises a temperature from 200°C to 500°C, and a pressure from 1 Torr to 100 Torr.

17. The method of claim 1 wherein the treating is for at least 1 second.

18. The method of claim 1 wherein the treating is for at least 10 seconds.

19. The method of claim 1 wherein the inner metal surface comprises an elemental metal or an alloy of elemental metals.

20. The method of claim 19 wherein the inner metal surface comprises tungsten.

21. The method of claim 1 wherein the inner metal surface comprises a conductive metal compound.

22. The method of claim 21 wherein the inner metal surface comprises TiN.

23. The method of claim 1 wherein the second capacitor electrode consists essentially of metal.

24. The method of claim 1 wherein the treating is effective to reduce leakage current of the capacitor than would otherwise occur in the absence of said treating.

25. The method of claim 1 wherein the exposed oxide surface comprises OH groups, the treating being effective to passivate said OH groups.

26. The method of claim 1 wherein the depositing the second capacitor electrode comprises using a halogen containing gas, the treating being effective to reduce halogen incorporation into the capacitor dielectric region than would otherwise occur in the absence of said treating.

27. The method of claim 1 wherein,

forming the capacitor dielectric region comprises deposition of multiple dielectric layers; and

intermediate at least some of the dielectric layer depositions, treating an outer surface of the capacitor dielectric region being formed with at least one of a borane or a silane.

28. The method of claim 27 wherein the treating is with at least one borane.

29. The method of claim 27 wherein the treating is with at least one silane.

30. The method of claim 27 wherein the multiple dielectric layers comprise at least two different dielectric materials.

31. The method of claim 27 wherein the multiple dielectric layers are of the same dielectric material.

32. The method of claim 1 wherein the first capacitor electrode consists essentially of semiconductive material and the second capacitor electrode consists essentially of metal thereby forming an MIS capacitor.

33. The method of claim 1 wherein the first capacitor electrode consists essentially of metal and the second capacitor electrode consists essentially of metal thereby forming an MIM capacitor.

34. A method of forming a capacitor, comprising:

forming a first capacitor electrode over a semiconductor substrate;

forming a capacitor dielectric region onto the first capacitor electrode, the capacitor dielectric region comprising an exposed oxide containing surface;

treating the exposed oxide containing surface of the capacitor dielectric region with at least one of a borane or a silane at a temperature from 200°C to 500°C and a pressure from 1 Torr to 100 Torr for at least 1 second, any layer deposited by the treating being no more than 3 monolayers thick; and

depositing a second capacitor electrode consisting essentially of metal over the treated oxide containing surface, the second capacitor electrode comprising an inner metal surface contacting against the treated oxide containing surface.

35. The method of claim 34 wherein the exposed oxide containing surface comprises hafnium oxide.

36. The method of claim 34 wherein the exposed oxide containing surface comprises aluminum oxide.

37. The method of claim 34 wherein the treating is with at least one borane.

38. The method of claim 37 wherein all borane used during the treating is void of halogen.

39. The method of claim 37 wherein the borane is selected from the group consisting of BH_3, B_2H_6, B_4H_{10}, B_5H_9, B_6H_{10} and $B_{10}H_{14}$, and mixtures thereof.

40. The method of claim 34 wherein the treating is with at least one silane.

41. The method of claim 40 wherein all silane used during the treating is void of halogen.

42. The method of claim 40 wherein the silane is selected from the group consisting of SiH_4, Si_2H_6, Si_3H_8 and Si_4H_{10}, and mixtures thereof.

43. The method of claim 34 wherein no layer is deposited by the treating.

44. The method of claim 34 wherein the treating is for at least 10 seconds.

45. The method of claim 34 wherein the inner metal surface comprises an elemental metal or an alloy of elemental metals.

46. The method of claim 45 wherein the inner metal surface comprises tungsten.

47. The method of claim 34 wherein the inner metal surface comprises a conductive metal compound.

48. The method of claim 47 wherein the inner metal surface comprises TiN.

49. The method of claim 34 wherein the treating is effective to reduce leakage current of the capacitor than would otherwise occur in the absence of said treating.

50. The method of claim 34 wherein the exposed oxide surface comprises OH groups, the treating being effective to passivate said OH groups.

51. The method of claim 34 wherein the depositing the second capacitor electrode comprises using a halogen containing gas, the treating being effective to reduce halogen incorporation into the capacitor dielectric region than would otherwise occur in the absence of said treating.

52. The method of claim 34 wherein,

forming the capacitor dielectric region comprises deposition of multiple dielectric layers; and

intermediate at least some of the dielectric layer depositions, treating an outer surface of the capacitor dielectric region being formed with at least one of a borane or a silane.

53. The method of claim 52 wherein the multiple dielectric layers comprise at least two different dielectric materials.

54. The method of claim 52 wherein the multiple dielectric layers are of the same dielectric material.

55. A method of forming a capacitor, comprising:

forming a first capacitor electrode over a semiconductor substrate, the first capacitor electrode comprising an exposed metal surface;

treating the exposed metal surface of the first capacitor electrode with at least one of a borane or a silane;

forming a capacitor dielectric region onto the first capacitor electrode, the capacitor dielectric region comprising an oxide containing surface received contacting against the treated metal surface of the first capacitor electrode; and

forming a second capacitor electrode over the capacitor dielectric region.

56. The method of claim 55 wherein the first capacitor electrode consists essentially of metal.

57. The method of claim 55 wherein the treating is with at least one borane.

58. The method of claim 55 wherein all borane used during the treating is void of halogen.

59. The method of claim 58 wherein the borane is selected from the group consisting of BH_3, B_2H_6, B_4H_{10}, B_5H_9, B_6H_{10} and $B_{10}H_{14}$, and mixtures thereof.

60. The method of claim 55 wherein the treating is with at least one silane.

61. The method of claim 60 wherein all borane used during the treating is void of halogen.

62. The method of claim 60 wherein the silane is selected from the group consisting of SiH_4, Si_2H_6, Si_3H_8 and Si_4H_{10}, and mixtures thereof.

63. The method of claim 55 wherein any layer deposited by the treating is no more than 3 monolayers thick.

64. The method of claim 63 wherein no layer is deposited by the treating.

65. The method of claim 55 wherein the treating comprises a temperature from 200°C to 500°C, and a pressure from 1 Torr to 100 Torr.

66. The method of claim 55 wherein the treating is for at least 1 second.

67. The method of claim 55 wherein the treating is for at least 10 seconds.

68. The method of claim 55 wherein the exposed metal surface comprises an elemental metal or an alloy of elemental metals.

69. The method of claim 55 wherein the exposed metal surface comprises a conductive metal compound.

70. The method of claim 55 wherein the second capacitor electrode consists essentially of metal.

71. The method of claim 55 wherein the second capacitor electrode consists essentially of semiconductive material.

72. The method of claim 55 wherein forming the capacitor dielectric region comprises using a halogen containing gas, the treating being effective to reduce halogen incorporation into the capacitor dielectric region than would otherwise occur in the absence of said treating.

73. The method of claim 55 wherein,

forming the capacitor dielectric region comprises deposition of multiple dielectric layers; and

intermediate at least some of the dielectric layer depositions, treating an outer surface of the capacitor dielectric region being formed with at least one of a borane or a silane.

74. The method of claim 73 wherein the treating is with at least one borane.

75. The method of claim 73 wherein the treating is with at least one silane.

76. The method of claim 73 wherein the multiple dielectric layers comprise at least two different dielectric materials.

77. The method of claim 73 wherein the multiple dielectric layers are of the same dielectric material.

78. The method of claim 55 wherein the first capacitor electrode consists essentially of metal and the second capacitor electrode consists essentially of semiconductive material thereby forming an SIM capacitor.

79. The method of claim 55 wherein the first capacitor electrode consists essentially of metal and the second capacitor electrode consists essentially of metal thereby forming an MIM capacitor.

80. A method of forming a capacitor, comprising:

forming a first capacitor electrode consisting essentially of metal over a semiconductor substrate, the first capacitor electrode comprising an exposed metal surface;

treating the exposed metal surface of the first capacitor electrode with at least one of a borane or a silane at a temperature from 200°C to 500°C and a pressure from 1 Torr to 100 Torr for at least 1 second, any layer deposited by the treating being no more than 3 monolayers thick.;

forming a capacitor dielectric region onto the first capacitor electrode, the capacitor dielectric region comprising an oxide containing surface received contacting against the treated metal surface of the first capacitor electrode; and

forming a second capacitor electrode over the capacitor dielectric region.

81. The method of claim 80 wherein the treating is with at least one borane.

82. The method of claim 80 wherein all borane used during the treating is void of halogen.

83. The method of claim 82 wherein the borane is selected from the group consisting of BH_3, B_2H_6, B_4H_{10}, B_5H_9, B_6H_{10} and $B_{10}H_{14}$, and mixtures thereof.

84. The method of claim 80 wherein the treating is with at least one silane.

85. The method of claim 84 wherein all silane used during the treating is void of halogen.

86. The method of claim 84 wherein the silane is selected from the group consisting of SiH_4, Si_2H_6, Si_3H_8 and Si_4H_{10}, and mixtures thereof.

87. The method of claim 80 wherein no layer is deposited by the treating.

88. The method of claim 80 wherein the treating is for at least 10 seconds.

89. The method of claim 80 wherein the exposed metal surface comprises an elemental metal or an alloy of elemental metals.

90. The method of claim 80 wherein the exposed metal surface comprises a conductive metal compound.

91. The method of claim 80 wherein forming the capacitor dielectric region comprises using a halogen containing gas, the treating being effective to reduce halogen incorporation into the capacitor dielectric region than would otherwise occur in the absence of said treating.

92. The method of claim 80 wherein,

forming the capacitor dielectric region comprises deposition of multiple dielectric layers; and

intermediate at least some of the dielectric layer depositions, treating an outer surface of the capacitor dielectric region being formed with at least one of a borane or a silane.

93. The method of claim 92 wherein the treating is with at least one borane.

94. The method of claim 92 wherein the treating is with at least one silane.

95. The method of claim 92 wherein the multiple dielectric layers comprise at least two different dielectric materials.

96. The method of claim 92 wherein the multiple dielectric layers are of the same dielectric material.